WHAT IS CLAIMED IS:

1. A data input unit of a synchronous semiconductor memory device comprising:

means for generating a rising edge signal and a falling edge signal at a rising edge and a falling edge of a data strobe signal DQS to be input;

means for generating a second falling edge signal whenever two prior falling edge signals are generated in response to the data strobe signal;

a data transforming means for dividing input data into four and latching the four divided data in response to the rising edge signal and the falling edge signal, and then latching again the four divided data in response to the second falling edge signal; and

a global input/output signal generator for transmitting the data from the data transforming means to a global input/output line in response to a strobe clock.

2. The data input unit of a synchronous semiconductor memory device according to claim 1, wherein the data transforming means comprises:

a first latch for latching input data in response to the rising edge signal;

a first latch group comprising a second latch and a third latch for latching input data latched by the first latch and new input data, respectively, in response to the falling edge signal;

a second latch group comprising a fourth latch, a fifth latch and a sixth latch for latching the respective input data latched by the second latch and the third latch, and new input data, respectively, in response to the rising edge signal;

a third latch group comprising a seventh latch, an eighth latch, a ninth latch and a tenth latch for latching the respective input data latched by the fourth latch, the fifth latch and the sixth latch, and new input data, respectively, in response to the falling edge signal; and

a fourth latch group comprising an eleventh latch, a twelfth latch, a thirteenth latch and a fourteenth latch for latching the respective input data latched by the seventh latch, the eighth latch, the ninth latch and the tenth latch, respectively, in response to the second falling edge signal.

3. The data input unit of a synchronous semiconductor memory device according to claim 1, wherein the strobe clock signal is applied to the global input/output signal generator during a period when data is latched in response to the second falling edge.

4. A data input method of a synchronous semiconductor memory device comprising the steps of:

latching input data in a first latch in response to a rising edge signal of a data strobe signal;

latching the input data latched in the first latch and new input data in a second latch and a third latch, respectively, in response to a falling edge signal of the data strobe signal;

latching the respective input data latched in the second latch and the third latch and new input data in a fourth latch, a fifth latch and a sixth latch, respectively, in response to the rising edge signal;

latching the respective input data latched in the fourth latch, the fifth latch and the sixth latch and new input data in a seventh latch, an eighth latch, a ninth latch and a tenth latch, respectively, in response to the falling edge signal;

latching the respective input data latched in the seventh latch, the eighth latch, the ninth latch and the tenth latch in an eleventh latch, a twelfth latch, a thirteenth latch and a fourteenth latch, respectively, in response to a second falling edge signal which is generated whenever two falling edge signals are generated in response to the data strobe signal; and

transmitting the respective input data latched in the eleventh latch, the twelfth latch, the thirteenth latch and the fourteenth latch to a global input/output line in response to a strobe clock.

5. The data input method of a synchronous semiconductor memory device according to claim 4, wherein the strobe clock signal is generated

during a period when the data is latched in response to the second falling edge signal.

6. A data input unit of a synchronous semiconductor memory device comprising:

a first signal generator producing a rising edge signal and a falling edge signal at a rising edge and a falling edge of a data strobe signal DQS to be input;

a second signal generator producing a second falling edge signal whenever two falling edge signals are generated by the first signal generator;

a latch network that divides input data into four, wherein the four divided data are latched in response to the rising edge signal and the falling edge signal, and wherein the four divided data are latched again in response to the second falling edge signal; and

a global input/output signal generator for transmitting the data from the data transforming means to a global input/output line in response to a strobe clock.

7. The data input unit of a synchronous semiconductor memory device according to claim 6, wherein the latch network comprises:

a first latch for latching input data in response to the rising edge signal;

a first latch group comprising a second latch and a third latch for latching input data latched by the first latch and new input data, respectively, in response to the falling edge signal;

a second latch group comprising a fourth latch, a fifth latch and a sixth latch for latching the respective input data latched by the second latch and the third latch, and new input data, respectively, in response to the rising edge signal;

a third latch group comprising a seventh latch, an eighth latch, a ninth latch and a tenth latch for latching the respective input data latched by the fourth latch, the fifth latch and the sixth latch, and new input data, respectively, in response to the falling edge signal; and

a fourth latch group comprising an eleventh latch, a twelfth latch, a thirteenth latch and a fourteenth latch for latching the respective input data latched by the seventh latch, the eighth latch, the ninth latch and the tenth latch, respectively, in response to the second falling edge signal.

8. The data input unit of a synchronous semiconductor memory device according to claim 6, wherein the strobe clock signal is applied to the global input/output signal generator during a period when data is latched in response to the second falling edge.